Ruiqi Chen

Master of Engineering | 1993/07 | Male
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Education

Ph.D. in Engineering Sciences, Vrije Universiteit Brussel, 2024-Now
M.S. in Integrated Circuit Engineering, Fuzhou University, 2017-2020, (Grade: A, Outstanding Graduate Award).
B.S. in Electronic Science and Technology, Southeast University Chengxian College, 2013-2017, (Grade: A).

Work Experience

Research Assistant, Southeast University **2023/07 – 2023/12**

Duties included: FPGA-based accelerator design for molecular docking and research article writing.

Supervisor: Professor Kun Wang

Research Assistant, Fudan University **2022/02 – 2023/02**

Duties included: FPGA-based graph neural networks accelerator design and research article writing.

Supervisor: Professor Kun Wang

Visiting Researcher, VeriMake Innovation-Lab **2020/06 – 2022/01**

Duties included: FPGA-based domain specific accelerator design and research article writing.

Supervisor: Mr. Yanxiang Zhu, Co-supervisor: Professor Ming Ling

Research Projects

FPGA-based Graph Neural Networks Accelerator Design **2022/02 - Present**

- An FPGA-based Overlay Processor is proposed for Graph Neural Networks (GNNs), facilitating rapid end-to-end software reconfiguration across diverse GNN model accelerators.
- Optimized designs for sparse matrix multipliers are presented, encompassing symmetric sparse matrix multipliers and high bandwidth general sparse matrix multipliers.
- **Publications**:

  [1]. "Graph-OPU: A Highly Integrated FPGA-Based Overlay Processor for Graph Neural Networks", in **FPL**, 2023.

  [2]. "Graph-OPU: An FPGA-Based Overlay Processor for Graph Neural Networks", in **FPGA**, 2023.

  [3]. "eSSpMV: An Embedded-FPGA-based Hardware Accelerator for Symmetric Sparse Matrix-Vector Multiplication," in **ISCAS**, 2023.

Hardware Accelerator for Computer-Aided Drug Design **2020/07 - Present**

- A hardware-accelerated approach for AutoDock Vina has been developed, leading to deployments on GPU and FPGA platforms with average speedups of 19.8x and 3.7x, respectively.
- An FPGA-based heterogeneous accelerator has been introduced for predicting GPCR ligand biological activity values. The system operates 54.5x faster than a CPU counterpart and achieves an energy efficiency that is 35.2x superior to GPU implementations.
- **Publications**:

  [1]. "FPGA Accelerating Multi-source Transfer Learning with GAT for Bioactivities of Ligands Targeting Orphan G Protein-coupled Receptors", in **FPL**, 2023.

  [2]. "Vina-FPGA: A Hardware-Accelerated Molecular Docking Tool With Fixed-Point Quantization and Low-Level Parallelism," **IEEE Trans. VLSI. Syst**, 2023.

  [3]. "Accelerating AutoDock Vina with GPUs," **Molecules**, 2022

Skills

- **Programming**: Verilog, VHDL, HLS, Python, C/C++
- **EDA Software**: Xilinx Vivado, Xilinx Vitis, Intel Quartus, Modelsim
- **Embedded Prototyping**: Android, Arduino, STM32 MCU, Raspberry Pi, Jetson

Selected Publications

· **FPGA-Based Approximate Multiplier for FP8**

Ruiqi Chen, Yangxintong Lyu, Hanbao, Jiayu Liu, Yanxiang Zhu, Shidi Tang, Ming Ling and Bruno da Silva

2025 IEEE 33rd Annual International Symposium on Field-Programmable Custom Computing Machines (**FCCM**)

(acceptance ratio: 20%)

· **ATE-GCN: An FPGA-based Graph Convolutional Network Accelerator with Asymmetrical Ternary Quantization**

Ruiqi Chen, Jiayu Liu, Shidi Tang, Yang Liu, Yanxiang Zhu, Ming Ling and Bruno da Silva

2025 Design, Automation & Test in Europe Conference & Exhibition (**DATE**) (acceptance ratio: 25%)

· **Vina-FPGA-Cluster: Multi-FPGA Based Molecular Docking Tool with High-Accuracy and Multi-Level Parallelism**

Ming Ling, Zhihao Feng, **Ruiqi Chen***, Yi Shao, Shidi Tang, and Yanxiang Zhu (*Corresponding authors)

IEEE Transactions on Biomedical Circuits and Systems, 2024, 18(6): 1321-1337.

· **FPGA-Based Sparse Matrix Multiplication Accelerators: From State-of-the-art to Future Opportunities**

Yajing Liu, **Ruiqi Chen**, Shuyang Li, Jing Yang, Shun Li and Bruno da Silva

ACM Transactions on Reconfigurable Technology and Systems, 2024, 17(4), Article 59 (November 2024): 1-37.

· **S-LGCN: Software-Hardware Co-Design for Accelerating LightGCN**

Shun Li, **Ruiqi Chen**, Enhao Tang, Yajing Liu, Jing Yang, and Kun Wang

2024 Design, Automation & Test in Europe Conference & Exhibition (**DATE**) (acceptance ratio: 24%).

· **Graph-OPU: A Highly Integrated FPGA-Based Overlay Processor for Graph Neural Networks**

Ruiqi Chen, Haoyang Zhang, Shun Li, Enhao Tang, Jun Yu and Kun Wang

2023 33rd International Conference on Field-Programmable Logic and Applications (**FPL**) (acceptance ratio: 24%)

· **FPGA Accelerating Multi-source Transfer Learning with GAT for Bioactivities of Ligands Targeting Orphan G Protein-coupled Receptors**

Ruiqi Chen, Haoyang Zhang, Jun Yu and Kun Wang

2023 33rd International Conference on Field-Programmable Logic and Applications (**FPL**) (acceptance ratio: 24%)

· **eSSpMV: An Embedded-FPGA-based Hardware Accelerator for Symmetric Sparse Matrix-Vector Multiplication**

Ruiqi Chen, Haoyang Zhang, Yuhanxiao Ma, Jianli Chen, Jun Yu, and Kun Wang

2023 IEEE International Symposium on Circuits and Systems (**ISCAS**)

· **Edge FPGA-based Onsite Neural Network Training**

Ruiqi Chen, Haoyang Zhang, Yu Li, Runzhou Zhang, Guoyu Li, Jun Yu, and Kun Wang

2023 IEEE International Symposium on Circuits and Systems (**ISCAS**)

· **Vina-FPGA: A Hardware-Accelerated Molecular Docking Tool With Fixed-Point Quantization and Low-Level Parallelism**

Ming Ling, Qingde Lin, **Ruiqi Chen***, Haimeng Qi, Mengru Lin, Yanxiang Zhu, Jiansheng Wu (*Corresponding authors)

IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023, 31(4): 484-497.

· **Accelerating AutoDock VINA with GPUs**

Tang, Shidi, **Ruiqi Chen**, Mengru Lin, Qingde Lin, Yanxiang Zhu, Ji Ding, Haifeng Hu, Ming Ling, and Jiansheng Wu.

Molecules, 2022, 27(9): 3041.

For more information, please visit my **website**.